ABSTRACT

An FPU pipeline is synchronized with a CPU pipeline. Synchronization is achieved by having stalls and freezes in any one pipeline cause stalls and freezes in the other pipeline as well. Exceptions are kept precise even for long floating point operations. Precise exceptions are achieved by having a first execution stage of the FPU pipeline generate a busy signal, when a first floating point instruction enters a first execution stage of the FPU pipeline. When a second floating point instruction is decoded by the FPU pipeline before the first floating point instruction has finished executing in the first stage of the FPU pipeline, then both pipelines are stalled.